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Design and implementation of 4-bit flash ADC using folding technique in cadence tool

Panchal S D[1], Dr. S S Gajre[2], Prof. V P Ghanwat[3]

SGGS Institute of Engineering and Technology,
Nanded, Maharashtra, India

er.spanchal@gmail.com,suhasgajre@gmail.com,vpghanwat@rediffmail.com,

ABSTRACT—***In this paper, we design a pipelined flash Analog-to- Digital Converter (ADC) to achieve high speed using 0.18umCMOS technology. The results obtained are also presented here. The physical circuit is more compact than the previous design.Power, processing time, and area are all minimized. This design can be used for modem high speed ADC applications.***

Keywords*—*CMOS comparator, CMOS Analog IntegratedCircuit, Flash Converter, priority encoder.

I. INTRODUCTION

The trend toward increased integration of analog and digital circuitry requires that data converters be embeddedin large digital ICs. Mixed-signal applications such as partialresponse maximum-likelihood (PRML) read channels and Gigabit Ethernet require high-speed low-resolution ADCs which are usually implemented with the flash architecture. By their nature, these applications rely heavily on DSP, which performs best when implemented on the finest geometry CMOS process. On the other hand, ADCs, as with analog circuits in general, tend to function best when fabricated on more mature CMOS.

Comparators are the key analog building block of any flash ADC and strongly influence performance. A high degree of comparator accuracy is essential for good ADC performance. However, integration of analog circuitry in low-voltage scale VLSI technologies results in degraded precision due to large device mismatch and limited voltage swing. Reduced precision can be compensated for through the use of offset correctionschemes. Analog offset correction techniques are typically used, but these schemes are increasingly difficult to implement in modern CMOS processes. For this reason, the issue of comparator offset is becoming a bottleneck in the design of flash ADCs.

This work focuses on reducing the amount of analog design and analog circuitry in a flash ADC. In particular, a flash ADCscheme was developed which tolerates low precision comparators. Much of the signal processing within the ADC has been transferred from the analog domain to the digital domain. In essence, digital techniques are used to compensate for the analog non-idealities. This alleviates the problem of difficult analog design, while harnessing the enhanced performance of digital circuits. The remaining analog components have "digital" accuracy requirements

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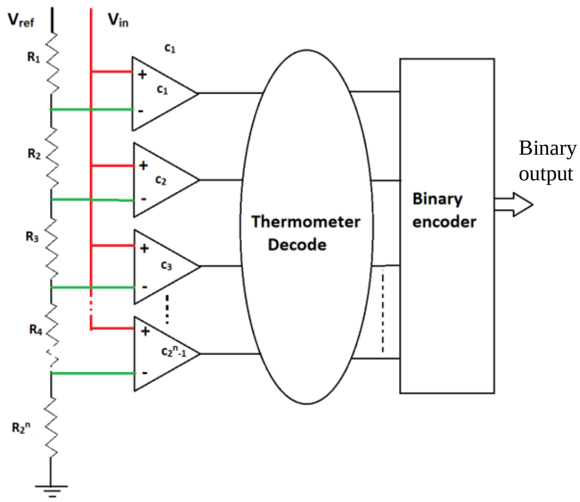

Fig.1. Conventional flash ADC.

A block diagram of a traditional flash ADC is shown in Fig. 1. An -bit converter has comparators. The nominal trip point of each comparator is set by a resistor ladder. Ideally, the comparator outputs form a thermometer code. The position of the meniscus (i.e., the 1–0 transition) represents the analog input and is determined by a thermometer decode circuit. The thermometer decode block generates a "1 of n" code which is converted to binary.

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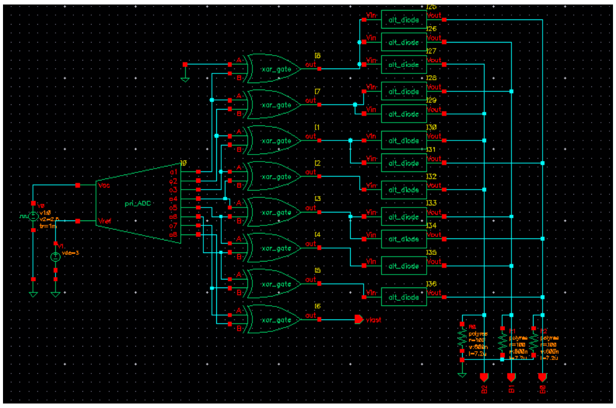

Fig. 2 schematics of flash ADC

As shown in Fig. 2, 3-bit ADC consists of 7 comparatorswhich the key analog building blocks of any flash ADC and strongly influence performance.

II. Design of Two Stage Comparator

A simple CMOS comparator is employed as shown in Fig. 3. Due to the verylow matching requirements, the comparator was optimized formaximum speed with minimum power and area.The comparator outputs no longer form a thermometer code.

DC balance condition for two stage comparator is given below,

Try to keep all devices in saturation - more gain and wider signalswings.

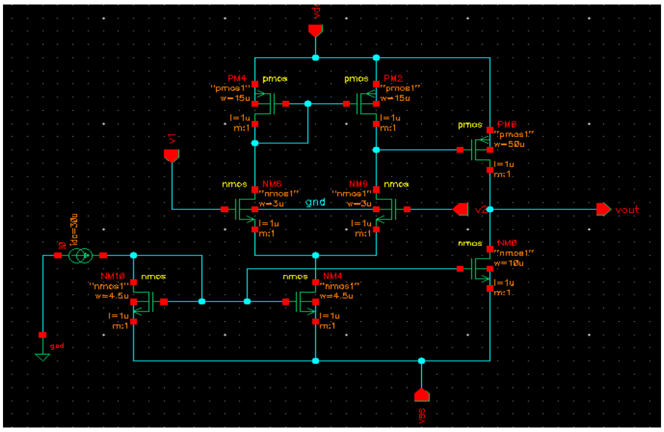

Fig.3 schematic of OP-AMP

Based on gate-source and DC current relationship i.e. if NM6 and NM9 are two matched devices and if $V_{GS\_NM6} = V_{GS\_NM9}$, then $I_{D\_NM6} = I_{D\_NM9}$ or viceversa.

Let $S_{NM6} = W_{NM6}/L_{NM6}$,

NM6 and NM9 matched gives $S_{NM6} = S_{NM9}$.

PM4 and PM2 matched gives $S_{PM4} = S_{PM2}$.

also, $I_{NM6} = I_{NM9} = 0.5I_{PM0}$.

From gate-source matching, we have $V_{GS\_NM4} = V_{GS\_NM0}$,

$I_{NM0} = I_{NM4}(S_{NM0}/S_{NM4})$ and $I_{PM0} = I_{PM2}(S_{PM0}/S_{PM2})$

Assume

$$V_{GS\_PM2} = V_{GS\_PM0}$$

For balance conditions, I_{PM0} must be equal to I_{NM0}, thus

$$(I_{NM4}/I_{PM2}).(S_{NM0}/S_{NM4}) = S_{PM0}/S_{PM2}$$

Since $I_{NM4}/I_{PM2} = 2$, then DC balance is achieved under the following:

$S_{PM0}/S_{PM2} = 2.(S_{NM0}/S_{NM4})$, $V_{DG\_PM2} = 0$,PM2 is saturated.

In Fig. 4, output of the trip-points of comparators 4 and 5 is 1 and 0 respectively which produces 1 as a output. The comparator outputsto form a thermometer code—as in Fig. 4. A standard encodermay then be used to complete the encoding process. Thisapproach requires a large switching matrix which has large areaand power requirements.

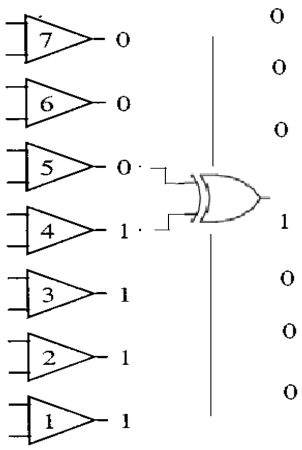

Fig. 4 converting thermometer code

III. Design of Xor Gates

While designing X-OR gate, We tried to reduce the number of transistors required to implement X-OR gate. And it is possible using ratioed logic. In ratioed logic, the PDN is replaced with a single unconditional load device that pulls up the output to Vod,

The aim is to be reducing number of MOS devices as well as optimize the power consumption. Due to ratioed logic, the number transistors are reduced N+1 while if we consider complementary CMOS could have reduced $2N_1$ transistors.

The nominal high output voltage(V_{OH}) for this gate V_{DD} because of PDN network is turned off and for nominal low output voltage in not 0v(V_{02}) because when there is PDN is on then also PMOS is on. As the result the noise margin and static power dissipation.

The output voltage and overall functionally it depend on the ratio of PMOS and NMOS sizes.

The V_{OL} is obtained by equating the currents through the load device & PDN for $V_{in}=V_{DD}$. Assuming PDN is in linear mode (i.e. output is close to 0v), while PMOS load is saturated,

$$K_n((V_{DD}-V_{Tn})V_{OL}-V^2_{OL}/2)+((-V_{DD}-V_{TP})V_{PSATP}-V_{PSATP}/2)=0$$

Consider $V_{OL} << (V_{DD}-V_T)$ &
$V_{TH}=V_{Tp}$

We can rewrite above equation as,

$$K_n((V_{DD}-V_{Tn})V_{OL})-K_P(V_{DD}+V_{T0})V_{SATp}-V^2_{DSATp}/2=0$$

$$K_n(V_{DD}-V_{Tn})V_{OL}=K_p(V_{DD}+V_{Tp})V_{DSATp}$$

IV. FOLDING TECHNIQUE

While optimizing circuit of ADC, we must consider the size of circuit which is biggest disadvantage of flash ADCs. To overcome this we have implemented logic circuit which requires minimum MOSFETS to increase bit size of ADC. This can be done by dividing amplitude of analog signal in to equal parts and applying 3-bit ADC encoder to output. This will convert two different analog signals into digital output.

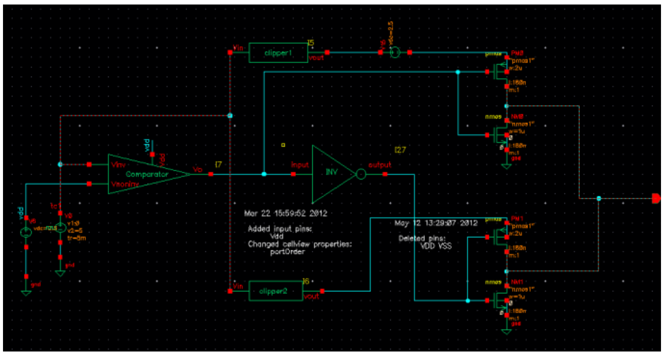

Fig. 5 Schematics of folding technique

As shown in Fig. 5 of logic circuit which divides the amplitude of analog signal in two different digital signals. Dividing amplitude can be done by two different clippers. Clipper 1 is used to clip amplitude below 2.5V while clipper2 is used clip amplitude above 2.5V. Also we included one voltage source after clipper1 which is used to shift entire signal to ground level.

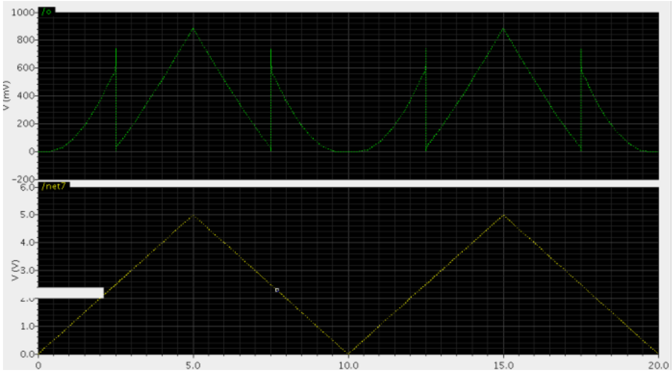

Fig. 6 output waveform of folding technique in flash ADC

Fig. 6 shows the output waveform of folding technique in which the voltage level above 2.5V is shifted down by using voltage level shifter.

V. COMPARISON

An ideal ADC has a great many bits for very fine resolution, samples at lightning-fast speeds, and recovers from steps instantly. It also, unfortunately, doesn't exist in the real world. Of course, any of these traits may be improved through additional circuit complexity, either in terms of increased component count and/or special circuit designs made to run at higher clock speeds.

Simple n-bit flash ADC requires 2^n-1 number of comparators i. e. for increasing accuracy and resolution we need to increase number of bits to represent signal into its digital form. For every increase in bit, number of comparators gets doubles.

For example 3-bit flash ADC we need 7 comparators and for 4-bit we need 15 comparators, but flash ADC using advance logic, we need only half of comparators. We get same output using less number of MOSFETS.

VI. CONCLUSION

An ADC designed and the circuit isoptimized with respect to time, power, and area consideringall the sub-micron effects. The output waveforms of theComparator, Encoder and the flash A/D Converter wereplotted and the desired values were obtained.

Some result are shown below in table

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Table 1: Specification of flash ADC

Parameter	value
Technology	180nm
Gain	72.5 dB at 150Hz 14.1 dB at 100MHz
Bandwidth	2.511E6 Hz
Power Supply	2.5 v

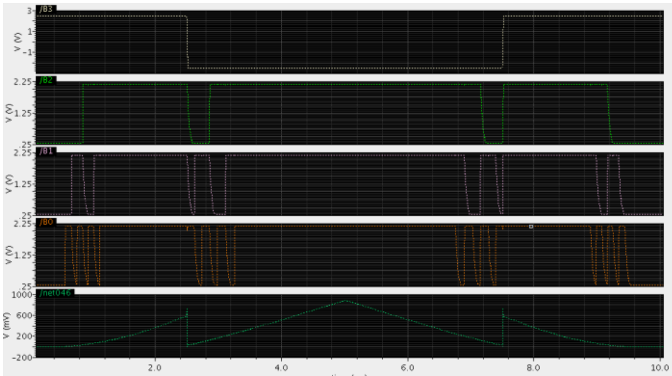

Fig. 7 Final result of flash ADC using Folding technique

As shown in above Fig. 7 we can observe that the final result consists of 4-bit digital signal and a folded analog signal. Initially we folded the analog signal into two parts in which first part is a signal below 2.5V, and second part is a signal above 2.5V.

ACKNOWLEDGMENT

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Biography

Panchal Sachin completed B.E. Electronics and Telecommunication in 2009 from M.G.Ms college of engineering, Nanded. Currently he is pursuing MTech. Electronics from SGGSIE&T and completing project using cadence tool, Nanded. He is interested in VLSI Design and Embedded System Design.

Dr.S SGajre currently is Professor in Electronics and Telecommunication department. He is B. E. Electronics from SGGS College of Engineering and Technology, Nanded in the year 1990. second rank in the University. He completed M.E. Electronics from SGGS College of Engineering and Technology, Nanded in the year 1994. He received Ph. D. in biomedical engineering from Indian Institute of Technology, Delhi.